

CLAIMS

What is claimed is:

1) A dual-port read SRAM cell for reducing soft errors comprising:

- 2 a) a cross-coupled latch, the cross-coupled latch having an input/output, and
 an input;
- 4 b) a first transfer device, the first transfer device having an input, a control
 input, and a output;
- 6 c) a second transfer device, the second transfer device having an input, a
 control input, and a output;
- 8 d) a third transfer device, the third transfer device having an input, a control
 input, and a output;
- 10 e) a fourth transfer device, the fourth transfer device having an input, a
 control input, and a output;
- 12 f) a first pull-down device, the first pull-down device having an input, a
 control input, and a output;
- 14 g) a second pull-down device, the second pull-down device having an input, a
 control input, and a output;
- 16 h) a third pull-down device, the third pull-down device having an input, a
 control input, and a output;
- 18 i) wherein the input/output of the cross-coupled latch is connected to the
 input of the fourth transfer device, the control input of the fourth transfer
20 device is connected to a third bitline, and the output of the fourth transfer
 device is connect to the output of the third pull-down device;

- 22 j) wherein the control input of the third pull-down device is connected to a
third wordline, and the input of the third pull-down device is connected to
24 ground;
- 26 k) wherein the input of the cross-coupled latch is connected to the output of
the first transfer device, the control input of the first transfer device is
connected to a first wordline, and the input of the first transfer device is
28 connected to a first bitline;
- 30 l) wherein the input/output of the cross-coupled latch is connected to the
control inputs of the first and second pull-down devices;
- 32 m) wherein the output of the first pull-down device is connected to the input
of the second transfer device, the control input of the second transfer
device is connected to a second wordline, and the output of the second
34 transfer device is connected to a second bitline;
- 36 n) wherein the output of the second pull-down device is connected to the
input of the third transfer device, the control input of the third transfer
device is connected to the first wordline, and the output of the third
38 transfer device is connected to the first bitline;
- 40 o) wherein the first inputs of the first and second pull-down devices are
connected to ground.

2) The dual-port read SRAM cell as in Claim 1 wherein the cross-coupled latch
2 comprises:

- 4 a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- c) a first NFET, the first NFET having a gate, a drain and a source;

- 6 d) a second NFET, the second NFET having a gate, a drain and a source;
- e) wherein the sources of the first and second PFETs are connected to VDD;
- 8 f) wherein the sources of the first and second NFETs are connected to GND;
- g) wherein the drain of the first PFET, the drain of the first NFET, the gate of
- 10 the second PFET and the gate of the second NFET are connected to the
- input/output of the cross-coupled latch;
- 12 h) wherein the drain of the second PFET, the drain of the second NFET, the
- gate of the first PFET and the gate of the first NFET are connected to the
- 14 input of the cross-coupled latch.

16

3) The dual-port read SRAM cell as in Claim 2 wherein:

- 2 a) the first transfer device comprises a third NFET such that the drain of the third
- NFET is connected to the output of the first transfer device, the gate of the
- 4 third NFET is connected to the control input of the first transfer device, and
- the source of the third NFET is connected to the input of the first transfer
- 6 device;
- b) the second transfer device comprises a fourth NFET such that the source of the
- 8 fourth NFET is connected to the input of the second transfer device, the gate
- of the fourth NFET is connected to the control input of the second transfer
- 10 device, and the drain of the fourth NFET is connected to the output of the
- second transfer device;
- 12 c) the third transfer device comprises a fifth NFET such that the source of the
- fifth NFET is connected to the input of the third transfer device, the gate of the
- 14 fifth NFET is connected to the control input of the third transfer device, and

the drain of the fifth NFET is connected to the output of the third transfer
16 device;

d) the fourth transfer device comprises a sixth NFET such that the drain of the
18 sixth NFET is connected to the input of the fourth transfer device, the gate of
the sixth NFET is connected to the control input of the fourth transfer device,
20 and the source of the sixth NFET is connected to the output of the fourth
transfer device.

22

4) The dual-port read SRAM cell as in Claim 3 wherein:

2 a) the first pull-down device comprises a seventh NFET such that the drain of the
seventh NFET is connected to the output of the first pull-down device, the gate
4 of the seventh NFET is connected to the control input of the first pull-down
device, and the source of the seventh NFET is connected to the input of the
6 first pull-down device;

b) the second pull-down device comprises an eighth NFET such that the drain of
8 the eighth NFET is connected to the output of the second pull-down device,
the gate of the eighth NFET is connected to the control input of the second
10 pull-down device, and the source of the eighth NFET is connected to the input
of the second pull-down device;

12 c) the third pull-down device comprises a ninth NFET such that the drain of the
ninth NFET is connected to the output of the third pull-down device, the gate
14 of the ninth NFET is connected to the control input of the third pull-down
device, and the source of the ninth NFET is connected to the input of the third
16 pull-down device.

5) The dual-port read SRAM cell as in Claim 1 wherein the input of the first transfer
2 device is a write-only port.

6) The dual-port read SRAM cell as in Claim 1 wherein the output of the second
2 transfer device and the output of the third transfer device are read-only ports.

7) The dual-port read SRAM cell as in Claim 6 wherein the input of the first transfer
2 device is a write-only port.

8) A method for manufacturing a dual-port read SRAM cell with improved soft error
2 rate comprising:

- a) fabricating a cross-coupled latch, the cross-coupled latch having an
4 input/output, and an input;
- b) fabricating a first transfer device, the first transfer device having an input, a
6 control input, and a output;
- c) fabricating a second transfer device, the second transfer device having an
8 input, a control input, and a output;
- d) fabricating a third transfer device, the third transfer device having an input, a
10 control input, and a output;
- e) fabricating a fourth transfer device, the fourth transfer device having an input,
12 a control input, and a output;
- f) fabricating a first pull-down device, the first pull-down device having an
14 input, a control input, and a output;
- g) fabricating a second pull-down device, the second pull-down device having an
16 input, a control input, and a output;

- h) fabricating a third pull-down device, the third pull-down device having an
18 input, a control input, and a output;
- i) wherein the input/output of the cross-coupled latch is connected to the input of
20 the fourth transfer device, the control input of the fourth transfer device is
connected to a third bitline, and the output of the fourth transfer device is
22 connect to the output of the third pull-down device;
- j) wherein the control input of the third pull-down device is connected to a third
24 wordline, and the input of the third pull-down device is connected to ground;
- k) wherein the input of the cross-coupled latch is connected to the output of the
26 first transfer device, the control input of the first transfer device is connected
to a first wordline, and the input of the first transfer device is connected to a
28 first bitline;
- l) wherein the input/output of the cross-coupled latch is connected to the control
30 inputs of the first and second pull-down devices;
- m) wherein the output of the first pull-down device is connected to the input of
32 the second transfer device, the control input of the second transfer device is
connected to a second wordline, and the output of the second transfer device is
34 connected to a second bitline;
- n) wherein the output of the second pull-down device is connected to the input of
36 the third transfer device, the control input of the third transfer device is
connected to the first wordline, and the output of the third transfer device is
38 connected to the first bitline;
- o) wherein the first inputs of the first and second pull-down devices are
40 connected to ground.

9) The method as in Claim 8 wherein the cross-coupled latch comprises:

- 2 a) a first PFET, the first PFET having a gate, a drain and a source;
- b) a second PFET, the second PFET having a gate, a drain and a source;
- 4 c) a first NFET, the first NFET having a gate, a drain and a source;
- d) a second NFET, the second NFET having a gate, a drain and a source;
- 6 e) wherein the sources of the first and second PFETs are connected to VDD;
- f) wherein the sources of the first and second NFETs are connected to GND;
- 8 g) wherein the drain of the first PFET, the drain of the first NFET, the gate of the
second PFET and the gate of the second NFET are connected to the
10 input/output of the cross-coupled latch;
- h) wherein the drain of the second PFET, the drain of the second NFET, the gate
12 of the first PFET and the gate of the first NFET are connected to the input of
the cross-coupled latch.

14

10) The method as in Claim 9 wherein:

- 2 a) the first transfer device comprises a third NFET such that the drain of the
third NFET is connected to the output of the first transfer device, the gate of
4 the third NFET is connected to the control input of the first transfer device,
and the source of the third NFET is connected to the input of the first transfer
6 device;
- b) the second transfer device comprises a fourth NFET such that the source of
8 the fourth NFET is connected to the input of the second transfer device, the
gate of the fourth NFET is connected to the control input of the second

10 transfer device, and the drain of the fourth NFET is connected to the output of
the second transfer device;

12 c) the third transfer device comprises a fifth NFET such that the source of the
fifth NFET is connected to the input of the third transfer device, the gate of the
14 fifth NFET is connected to the control input of the third transfer device, and
the drain of the fifth NFET is connected to the output of the third transfer
16 device;

d) the fourth transfer device comprises a sixth NFET such that the drain of the
18 sixth NFET is connected to the input of the fourth transfer device, the gate of
the sixth NFET is connected to the control input of the fourth transfer device,
20 and the source of the sixth NFET is connected to the output of the fourth
transfer device.

22

11) The method as in Claim 10 wherein:

2 a) the first pull-down device comprises a seventh NFET such that the
drain of the seventh NFET is connected to the output of the first pull-
4 down device, the gate of the seventh NFET is connected to the control
input of the first pull-down device, and the source of the seventh NFET
6 is connected to the input of the first pull-down device;

b) the second pull-down device comprises an eighth NFET such that the
8 drain of the eighth NFET is connected to the output of the second pull-
down device, the gate of the eighth NFET is connected to the control
10 input of the second pull-down device, and the source of the eighth
NFET is connected to the input of the second pull-down device;

12 c) the third pull-down device comprises an ninth NFET such that the
drain of the ninth NFET is connected to the output of the third pull-
14 down device, the gate of the ninth NFET is connected to the control
input of the third pull-down device, and the source of the ninth NFET
16 is connected to the input of the third pull-down device.

18

12) A dual-port read SRAM cell for reducing soft errors comprising:

- 2 a) a means for storing charge, the means for storing charge having an
input/output, and an input;
- 4 b) a first means for transferring charge, the first means for transferring charge
having an input, a control input, and a output;
- 6 c) a second means for transferring charge, the second means for transferring
charge having an input, a control input, and a output;
- 8 d) a third means for transferring charge, the third means for transferring
charge having an input, a control input, and a output;
- 10 e) a fourth means for transferring charge, the fourth means for transferring
charge having an input, a control input, and a output;
- 12 f) a first means for connecting a node to ground, the first means for
connecting a node to ground having an input, a control input, and a output;
- 14 g) a second means for connecting a node to ground, the means for connecting
a node to ground having an input, a control input, and a output;
- 16 h) a third means for connecting a node to ground, the third means for
connecting a node to ground having an input, a control input, and a output;

- 18 i) wherein the input/output of the means for storing charge is connected to
the input of the fourth means for transferring charge, the control input of
20 the fourth means for transferring charge is connected to a third bitline, and
the output of the fourth means for transferring charge is connect to the
22 output of the third means for connecting a node to ground;
- j) wherein the control input of the third means for connecting a node to
24 ground is connected to a third wordline, and the input of the third means
for connecting a node to ground is connected to ground;
- 26 k) wherein the input of the means for storing charge is connected to the
output of the first means for transferring charge, the control input of the
28 first means for transferring charge is connected to a first wordline, and the
input of the first means for transferring charge is connected to a first
30 bitline;
- l) wherein the input/output of the means for storing charge is connected to
32 the control inputs of the first and second means for connecting a node to
ground;
- 34 m) wherein the output of the first means for connecting a node to ground is
connected to the input of the second means for transferring charge, the
36 control input of the second means for transferring charge is connected to a
second wordline, and the output of the second means for transferring
38 charge is connected to a second bitline;
- n) wherein the output of the second means for connecting a node to ground is
40 connected to the input of the third means for transferring charge, the
control input of the third means for transferring charge is connected to the

42 first wordline, and the output of the third means for transferring charge is
connected to the first bitline;

44 o) wherein the first inputs of the first and second means for connecting a
node to ground are connected to ground.

46